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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,191	01/12/2005	Takashi Yokokawa	09812.0201	8642

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EXAMINER

RIZK, SAMIR WADIE

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/521,191	YOKOKAWA ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 1/12/05.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 January 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/12/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTIONS

- Claims 1-20 have been submitted for examination
- Claims 1-20 have been rejected

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

2. Figures (1-8) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 20 is rejected under 35 U.S.C. 101 because the claim invention is directed to non-statutory subject matter. Each limitation in claim 41 comprises an abstract

algorithm that can be carried by hand or computer software program element and is **not tangibly embodied**. Abstract algorithms are non-statutory. **Un-executed** Computer programs are non-statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 12 should read:

"..... the weight of the rows and columns of said check matrix **respectively**."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Richardson et al. US patent no. 6633856 (Hereinafter Richardson).
6. In regard to claim 1, Richardson teaches:
- A decoding method of decoding LDPC (Low Density Parity Check) codes, said decoding method comprising:
 - a decoding step of decoding said LDPC codes by using a transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix.

(Note: Abstract in Richardson)

7. In regard to claim 2, Richardson teaches:

- The decoding method according to Claim 1, wherein, by using, as a formation matrix, a $P \times P$ unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, shift matrix, and a $P \times P$ said quasi-unit matrix, and said 0-matrix, said transformation by a combination of a plurality check matrix is represented of said formation matrices.

(Note: Figure 13 and col. 21, lines (53-65) in Richardson)

8. In regard to claim 3, Richardson teaches:

- The decoding method according to Claim 1 further comprising:
- a code sequence permutation step of performing, on the code sequence of said received LDPC codes, the same column permutation as the column permutation performed on said original check matrix and outputting a permuted code sequence, wherein, in said decoding step, said code sequence is decoded by using said transformation check matrix and said permuted code sequence.

(Note: col. 22, lines (50-55) in Richardson)

9. In regard to claim 4, Richardson teaches:

- A decoding apparatus for decoding LDPC (Low Density Parity Check) codes, said decoding apparatus comprising:

- decoding means for decoding said LDPC codes by using a transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix.

(Note: Abstract in Richardson)

10. In regard to claim 5, Richardson teaches:

- The decoding apparatus according to Claim 4 wherein, by using, as a formation matrix, a unit matrix, a quasi-unit matrix which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said shift matrix, and a $P \times P$ O-matrix, said transformation check matrix is represented by a combination of a plurality of said formation matrices.

(Note: Figure 13 and col. 21, lines (53-65) in Richardson)

11. In regard to claim 6, Richardson teaches:

- The decoding apparatus according to Claim 5, wherein said decoding means comprises:
- check node calculation means for simultaneously performing p check node computations for decoding said LDPC codes; and
- variable node calculation means for simultaneously performing p variable node computations for decoding said LDPC codes.

(Note: Figure 9, reference sign (906) and col. 21, lines (44-47) in Richardson)

12. In regard to claim 7, Richardson teaches:

- The decoding apparatus according to Claim 6, wherein said check node calculation means comprises p check node calculators for performing computations of check nodes, and said variable node calculation means comprises p variable node calculators for performing computations of variable nodes.

(Note: Col.23, lines (35-45) in Richardson)

13. In regard to claim 8, Richardson teaches:

- The decoding apparatus according to Claim 6, wherein said decoding means further comprises message storage means for simultaneously reading and writing message data corresponding to p edges obtained as a result of said computations of the p check nodes or the p variable nodes.

(Note: Figure 9, reference sign (906) and col. 21, lines (44-47) in Richardson)

14. In regard to claim 9, Richardson teaches:

- The decoding apparatus according to Claim 8, wherein said message storage means stores message data corresponding to the edges which are read during a check node computation in such a manner that 1s of

said transformation check matrices are padded closer in the row direction.

(Note: Col. 21, lines (39-65) in Richardson)

15. In regard to claim 10, Richardson teaches:

- The decoding apparatus according to Claim 8, wherein said message storage means stores message data corresponding to the edges which are read during a variable node computation in such a manner that 1s of said transformation check matrix is padded closer in the column direction.

(Note: Figure 8, sing (806) and col.15, lines (52-65) in Richardson)

16. In regard to claim 11, Richardson teaches:

- The decoding apparatus according to Claim 8, wherein said message storage means stores, at the same address, messages corresponding to p edges belonging to a unit matrix, a quasi-unit matrix, or a shift matrix whose weight is 1 when the formation matrices, whose weight is or more, representing said transformation check matrix are represented in the form of the sum of the unit matrix, the quasi-unit matrix, or the shift matrix, whose weight is 1.

(Note; col. 22, lines (35-40) in Richardson)

17. In regard to claim 12, Richardson teaches:

- The decoding apparatus according to Claim 8, wherein said message storage means comprises number-of-the-rows/p FIFOs and number-of-

the-columns/p FIFOs, and said number-of-the-rows/p FIFOs and said number-of-the-columns/p FIFOs each have a number of words corresponding to the weight of the rows and columns of said check matrix.

(Note: col. 20, line 44 in Richardson)

18. In regard to claim 13, Richardson teaches:

- The decoding apparatus according to Claim 8, wherein said message storage means comprises a RAM (Random Access Memory), and said RAM stores said message data in such a manner as to be padded closer in the read-out sequence and reads said message data in the storage position sequence.

(Note: Figure 15, reference sign (1506) and col. 23, lines (8-10) in Richardson)

19. In regard to claim 14, Richardson teaches:

- The decoding apparatus according to Claim 6, wherein said decoding means further comprises received information storage means for storing received information and simultaneously reading p pieces of the received information.

(Note: col. 21, lines (41-43) In Richardson)

20. In regard to claim 15, Richardson teaches:

- The decoding apparatus according to Claim 14, wherein said received information storage means stores said received information in such a

manner that said received information can be read in the sequence
necessary for said computations of variable nodes.

(Note: Figure 15, reference sign (1504) in Richardson)

21. In regard to claim 16, Richardson teaches:

- The decoding apparatus according to Claim 6, wherein said decoding means further comprises cyclic shift means for cyclically shifting messages obtained as a result of said p check node computations or said p variable node computations.

(Note: Figure 13 and col. 21, lines (53-65) in Richardson)

22. In regard to claim 17, Richardson teaches:

- The decoding apparatus according to Claim 16, wherein said cyclic shift means comprises a barrel shifter.

(Note: col.21, lines (52-65) in Richardson)

23. In regard to claim 18, Richardson teaches:

- The decoding apparatus according to Claim 4, further comprising code sequence permutation means for performing, on the code sequence of said received LDPC codes, the same column permutation as the column permutation performed on said original check matrix and outputting a permuted code sequence, wherein said decoding means decodes said code sequence by using said transformation check matrix and said permuted code sequence.

(Note: col. 22, lines (50-55) in Richardson)

24. In regard to claim 19, Richardson teaches:

- The decoding apparatus according to Claim 18, further comprising inverse permutation means for performing, on the output of said decoding means, an inverse permutation of a column permutation performed on said original check matrix, and for outputting a final decoded result.

(Note; claim 39 in Richardson)

25. In regard to claim 20, Richardson teaches:

- a program for enabling computer to decode LDPC (Low Density Parity Check) codes, said program comprising:
- a decoding step of decoding said LDPC codes by using a transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix.

(Note: Abstract in Richardson)

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Jin et al. US patent no. 6961888 teaches method and apparatus for encoding LDPC codes.
- Richardson et al. US publication no. US 2005/0278606 teaches method and apparatus for decoding LDPC codes.

- Richardson et al. US patent no. 6938196 teaches node processors for use in parity check decoders.
- Hocevar US publication no. US 2004/0034828 teaches Hardware efficient low density parity check code for digital communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

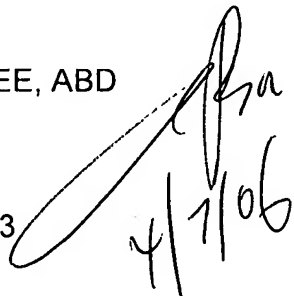
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133



GUY LAMARRE
PRIMARY EXAMINER